In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 27 and 28 without prejudice.

1. (Currently Amended) A computer system comprising a microprocessor having a dynamically re-configurable trace cache to provide application specific configuration of the trace cache, the trace cache including:

a tag array;

a data array; and

a next fetch address (NFA) array,

wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries.

2. (Currently Amended) The computer system of claim 1 wherein the microprocessor further comprises:

a fill unit to form micro-operations; and

branch prediction logic.

~~trace cache comprises:~~

~~a tag array;~~

~~a data array; and~~

~~a next fetch address (NFA) array.~~

3. (Currently Amended) The computer system of claim 2 wherein the microprocessor further comprises an execution core to execute the micro-operations ~~tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries~~.

4. (Currently Amended) The computer system of claim 1 ~~3~~ wherein each trace stored in the trace cache is assigned an index value.

5. (Original) The computer system of claim 4 wherein the tag array, the data array and the NFA array each comprise a decoder to access a trace stored in the one or more temporal address entries using an index value.

6. (Currently Amended) The computer system of claim 1 ~~3~~ wherein the one or more temporal address entries are generated by simulating to identify dynamic traces, the execution behavior of the dynamic traces and generating an index value for each identified trace.

7-15. (Canceled)

16. (Currently Amended) A microprocessor comprising:

an instruction cache to receive and store the micro-operations as cache lines; and

a trace cache, coupled to the instruction cache, that is dynamically re-configurable using profile information to provide application specific configuration of the trace cache, the trace cache including:

a tag array;

a data array; and

a next fetch address (NFA) array,

wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries.~~and an execution core to execute the micro-operations.~~

17. (Original) The microprocessor of claim 16 further comprising:

a fill unit to form micro-operations; and

branch prediction logic.

18. (Currently Amended) The microprocessor of claim 16 wherein the one or more temporal address entries are generated by simulating to identify dynamic traces, the execution behavior of the dynamic traces and generating an index value for each identified trace.~~trace cache comprises:~~

~~a tag array;~~

~~a data array; and~~

~~a next fetch address (NFA) array.~~

19. (Currently Amended) The microprocessor of claim ~~18~~ 16 further comprising an execution core to execute the micro-operations ~~wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries~~.

20. (Currently Amended) The microprocessor of claim ~~19~~ 16 wherein each trace stored in the trace cache is assigned an index value.

21. (Original) The microprocessor of claim 20 wherein the tag array, the data array and the NFA array each comprise a decoder to access a trace stored in the one or more temporal address entries using an index value.

22. (Original) A trace cache comprising:

a tag array;

a data array; and

a next fetch address (NFA) array;

wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries.

23. (Currently Amended) The trace cache ~~microprocessor~~ of claim 22 wherein each trace stored in the trace cache is assigned an index value.

24. (Currently Amended) The trace cache ~~microprocessor~~ of claim 23 wherein the tag array, the data array and the NFA array each comprise a decoder to access a trace stored in the one or more temporal address entries using an index value.

25. (Currently Amended) The trace cache ~~microprocessor~~ of claim 22 wherein the one or more temporal address entries are generated by simulating to identify dynamic traces, the execution behavior of the dynamic traces and generating an index value for each identified trace.

26. (Currently Amended) A computer system comprising:

a microprocessor having a dynamically re-configurable trace cache to provide application specific configuration of the trace cache, the trace cache including:

a tag array;

a data array; and

a next fetch address (NFA) array,

wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries;

a chipset coupled to microprocessor; and

a main memory coupled to the chipset.

27. (Cancelled)

28. (Cancelled)

29. (Currently Amended) The computer system of claim 26 ~~28~~ wherein each trace stored in the trace cache is assigned an index value.

30. (Original) The computer system of claim 29 wherein the tag array, the data array and the NFA array each comprise a decoder to access a trace stored in the one or more temporal address entries using an index value.